Title of the invention

A method for analyzing circuit pattern defects and a system thereof

Background of the invention

The present invention relates to a method for analyzing defects in electronic circuits produced by forming electronic circuit patterns, and a system thereof. More specifically, the present invention relates to a defect analysis technology for accurately evaluating electronic criticality of defects generated in intermediate processes and performing analysis with priority being given to critical defects having a high electronic criticality. In particular, the present invention provides a technology suitable for use in electronic circuit production where production takes place through multiple production processes such as in semiconductor devices.

Semiconductor device production involves hundreds of production processes and requires dozens of days from the start of wafer processing to completion. The object of each of the production processes is to provide proper electronic operation at completion. For this reason, it is important to discover critical defects that will lead to electronic faults upon completion at intermediate processes and to prevent these defects from being generated.

Japanese laid-open patent publication number Hei 11-176899 (the first conventional technology) describes a defect warning method and a defect warning system. When a testing process performed at the end of the wafer production process is reached, a consistency check is performed between coordinates of defects detected in inspections performed at intermediate processes and coordinates of faults defected in the testing process. The process and location of generation of critical defects leading to faults is determined in the testing process and an evaluation value is calculated. A warning is issued if the evaluation value exceeds a predetermined threshold value.

Japanese laid-open patent publication number Hei 8-21803 (the second

conventional technology) describes a defect type evaluation device. Defect images are captured at an intermediate process and defect information extracted from the defect images are provided as input to a neural processing unit. Defect types are obtained from the output. In this conventional technology, defects representative of different defect types are used as samples for preliminary training. The samples are prepared manually through observation and classification of defect images. Image characteristics extracted from the defect images through image processing are used for the defect information provided as input to the neural processing unit.

In the first conventional technology described above, critical defects cannot be evaluated until the semiconductor device is completed and the testing process is reached. As a result, there is a delay between when a defect is generated and when measures against further defects can be taken, making production of faulty products unavoidable. If critical defects are repeatedly generated at the same place on wafers, the coordinates obtained from inspections at intermediate processes can be used to detect generation of critical defects, but this applies only to these restricted cases.

In the second conventional technology, defects can be classified in intermediate processes into categories based on similar image characteristics. However, accurate classification of critical defects and non-critical defects is difficult. To accurately classify critical defects, the accurate preparation of samples used for training is important. However, preparing accurate critical defect samples for different types of defects generated in the production process through manual observation and classification is difficult. For example, with adhesion of contaminants on an electronic circuit pattern, not all contaminants will lead to a critical defect. The probability that a contaminant will lead to a short-circuit defect will vary greatly depending on whether the contaminant is formed from a conductive material or a non-conductive material. Also, the probability that a contaminant will lead to a short-circuit defect will vary depending on the relation between the height of the contaminant and the thickness of

the film forming the electronic circuit pattern. Information relating to the material and height of contaminants is difficult to identify through manual observation of defect images.

Summary of the invention

The object of the present invention is to overcome the problems described above and to clarify the relation between detailed defect information and electronic criticality based on objective data processing. The detailed information here refers to microscope images, SEM images, EDX analysis curves, and the like and will depend on the type of detecting device used. Another object of the present invention is to provide means for accurately evaluating electronic criticality of defects in intermediate processes by classifying defects based on this detailed information. With the present invention, generation of critical defects during intermediate processes can be detected accurately. By giving priority to critical defects when taking preventative measures, production of faulty products can be kept to a minimum.

In order to achieve the objects described above, the present invention provides a method for analyzing defects detected in the production process of an electronic circuit pattern as described below. A defect on the inspected object is detected, and the position information for this detected defect is stored. Detailed information on this defect is collected for this defect for which position information was stored. This collected detailed information is associated with the defect position information and stored. The inspected object is electronically tested, and information on positions at which faults are generated in this electronic test is stored. The stored defect position information and the fault-generating position information are compared, and the detected defect is classified based on the results of this comparison. Then, information relating to this classified defect is displayed.

In another aspect of the present invention, the present invention provides a

system for analyzing defects detected in the production process of an electronic circuit pattern as described below. First means for storing stores defect position information obtained by detecting defects on an inspected object. Second means for storing stores detailed information observed based on defect position information stored in first storing means in association with position information for this defect. Third means for storing stores information on positions of faults generated by an electronic test when the inspected object is electronically tested. Means for comparing compares the defect position information stored in second storing means with fault generating position information stored in third storing means. Means for classifying classifies detailed information stored in second storing means based on results from comparing means. Means for outputting outputs information relating to the detailed information classified by classifying means.

These and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

Brief description of the drawings

Fig. 1 is a block diagram showing the architecture of a defect analysis system according to an embodiment of the present invention.

Fig.2 shows a flowchart of image classification steps using training data.

Fig.3 is a drawing for the purpose of describing an example of a semiconductor device production process flow according to an embodiment of the present invention.

Fig.4 is a flowchart showing the sequence of operations performed in defect analysis according to a first embodiment of the present invention.

Fig.5 is a drawing for the purpose of describing examples of consistency checking operations.

Fig.6 is a drawing for the purpose of describing an example of how consistency checking results are stored.

Fig.7 is a drawing for the purpose of describing an example of a displayed defect image.

Fig.8 is an image of defect maps and defect images and so on displayed on a screen.

Fig.9 is a drawing for the purpose of describing an example where an image classification field is added to the storage fields from Fig.7.

Fig.10 is a cross-section drawing of dark contaminants and bright contaminants.

Fig.11 is a descriptive drawing showing examples of criticality rate calculations.

Fig.12 is a drawing for the purpose of describing an example of results from a semiconductor device production process.

Fig.13 is a drawing for the purpose of describing an example of sampling operations.

Fig.14 shows a concept of coordinate consistency checking operation.

Fig.15 shows an example of a sampling operation.

Description of the preferred embodiments

The embodiments of the present invention as applied to a production process for semiconductor devices will be described in detail below, with references to the figures.

Fig. 1 is a block diagram showing a defect analysis system architecture relating to a first embodiment of the present invention. As the figure shows, the defect analysis system of this embodiment includes an inspection device 100, a review device 101, an electronic tester 102, a defect management server 103, a classifying device 111,

and a network 104 connecting these elements. This figure shows one implementation of this invention, but it would also be possible to have, for example, the classifying device 111 equipped with the functions for a display device 109, an input device 110, and a storage device 108. Also, the classifying device 111 itself may be formed as a part of the defect data management server 103, the detection device 100, or the review device 101.

The following is a description of the flow of operations performed by the architecture shown in this figure, with references to Fig. 2. First, the inspection device 100 is used to perform a defect inspection of the wafer. When this inspection is completed, the review device 101 retrieves defect images 211 corresponding to defect coordinates 210 obtained from the defect inspection results and indicating positions of defects on the wafer. The associations between the images and the coordinates are stored in the storage device 108 by way of the defect data management server 103. Next, the electronic tester 102 performs an electronic test of the same wafer and determines fault coordinates 212 from the test. The defect data management server 103 performs a consistency check 213 between the defect coordinates 210 and the electronic testing fault coordinates 212. This operation allows the defect coordinates 210 to be classified into critical defects 214, which match the electronic test fault coordinates 212, and non-critical defects 215, which do not match. By using the associations between defect coordinates 210 and the defect images 211, the defect images 211 can be classified into a critical defects 214 group and a non-critical defects 215 group. Based on the results of this classification and using the defect images belonging to the critical defects 214 and the non-critical defects 215, the classification device 111 obtains training data 216, in which image characteristics are quantified. This training data 216 has a high correlation with the electronic test results. Furthermore, the classification device 111 can generate learned data 217, which contains parameters for converting image characteristics into categories, based on the

training data 216. This would allow an unknown image 218 detected by a different wafer defect inspection to be classified accurately into the critical defects 214 group or the non-critical defects 215 group.

The individual devices in the system will be described below.

The inspection device 100 detects positions on the wafer surface where contaminants and circuit pattern deformations are present and outputs the coordinate data for these positions. The inspection device 100 is formed from an automated stage, a detection optical system, a linear sensor, an image processing device, and the like. The inspection is performed as follows. A linear sensor disposed at the imaging position of a microscope in the detection optical system continuously captures images while the automated stage, on which a wafer is mounted, is moved. Images for positions at which identically shaped circuits are present are compared by the image processing device, and areas with different brightnesses are detected as defects. The coordinate data for these areas are output. Output coordinate data 105 is sent to the defect data management server 103 by way of the network 104.

The role of the inspection device 100 is to visually inspect circuit patterns to determine the number of critical defects that will lead to electronic faults during a process in which the electronic operation of the semiconductor device cannot be tested. By preventing critical defects from taking place, production of faulty products can be minimized and yield can be improved.

The review device 101 collects detailed information on the defects detected by the inspection device 100 and includes an automated stage, a detection system, a memory device, and the like. The detailed information can be optical microscope images, SEM images, EDX analysis curves, or the like and depends on the type of detection system used. The review device 101 operates as follows. The defect coordinate data 105 is received from the defect data management server 103 by way of the network 104. The automated stage on which the wafer is mounted is moved to the

defect position, and the detection system is used to collect detailed defect information, which is then stored in the memory device. The stored detailed information 106 is sent to the defect data management server 103 by way of the network 104.

The role of the review device 101 is to collect detailed information on the defects detected by the inspection device 100 to be used to select the critical defects. The defects detected by the inspection device 100 include coloration defects and contaminant defects, which are electronically functional and not critical defects, in addition to critical defects. Thus, critical defects need to be identified using the detailed defect information. Furthermore, another role of the review device 101 is to classify defects using the detailed information. This allows the primary mode of defects to be determined so that the causes can be identified.

Since the inspection device 100 can perform high-speed inspection over a wide area, collecting detailed information at the same time as performing inspection is difficult. The review device 101 is necessary because it allows detailed information to be collected by returning to the defect position. However, if detecting means in the inspection device 100 can be switched, the inspection device 100 can be equipped with the functions of the review device 101.

Since the number of defects for which detailed information can be collected by the review device 101 is limited by time factors, it is also possible to use the defect information output by the inspection device 100 during inspection in place of the detailed information. In this case, the amount of information in the defect information output by the inspection device 100 will be less than the detailed information collected by the review device 101, but the lack of a time delay allows general tendencies to be determined in a short period of time.

If the defect information output from the inspection device 100 in the present invention, the information can be treated in the same manner as the detailed information collected by the review device 101. Also, defects for which detailed

information is to be collected using the review device 101 can be selected based on the classification results of the defect information output from the inspection device 100.

The electronic tester 102 checks electronic operations after the semiconductor device is completed. The electronic tester 102 includes an automated stage, an electronic probe, an electronic circuit device, and the like. The electronic tester 102 operates as follows. The completed wafer is mounted on the automated stage and the electronic probe is successively positioned at individual chip positions. Potential is applied with the electronic probe placed in contact with the individual chip, and a test is performed using the electronic circuit device. For example, with a memory product, a map of failed bits, containing a detailed record of positions of faulty bits on the wafer, can be obtained. Test results 107 output from the electronic tester 102 are sent to the defect data management server 103 by way of the network 104 and are stored in the storage device 108.

The defect data management server 103 is a computer system connected to the network 104 and includes a CPU device, a memory device, a storage device 108, a display device 109, an input device 110, and the like. The server 103 sends and receives information to and from the inspection device 100, the review device 101, and the electronic tester 102. The server 103 is also equipped with data processing functions (sampling, coordinate consistency checking, image classifying, criticality evaluation, criticality checking) and serves as the key element of the present invention. The detailed operations of the defect data management server 103 will be described later.

The classifying device 111 is a computer system that visually classifies critical defects in an automated manner. The classifying device 111 passes data back and forth with the critical data management server 103, the inspection device 100, the review device 101, and the like, by way of the network 104.

The operations of the classifying device 111 will be described. A program

installed in the classifying device 111 uses a known pattern recognition method such as the one described in "Image Analysis Handbook" (Takaki, et al., Tokyo Daigaku Shuppankai, 1991, pp. 171-205, pp. 641-688). In this pattern recognition method, characteristics of a sample image set up beforehand are compared with the characteristics of an unknown image. The unknown image is classified based on similarities of characteristics. Using a defect image as an example, the characteristics can be numerical data relating to defect color (including brightness), size, and shape.

The classifying device 111 performs training operations and classifying operations. Training operations are performed using training data prepared by an operator. The training data is prepared by the operator, who studies defect images displayed on the display device 109 of the defect data management server 103 and selects sample images using the input device 110 or the like. The sample images and its classifications selected from the display device 109 are stored as the training data. This training data is transferred from the defect data management server 103 to the classifying device 111.

In the training operation, the characteristics of the sample image are extracted, and these characteristics and the training data are used to calculate parameters for converting characteristics to classifications. In the classifying operation, the characteristics of the unknown image transferred from the review device 101 are extracted, and a classification is determined using the conversion parameters generated in the training operation. The determined classification is stored in the storage device 108 in association with the defect image.

For the classifying device 111 to operate correctly, it is important that the sample image is correctly classified in the training step. In the classifying device 111, this is implemented using an ADC (Automatic Defect Classification) device. An example in which an ADC device is used in the present invention will be described in detail later.

Fig.3 shows an example in which the present invention is used in a semiconductor device production process. The defect analysis method of the present invention involves a preparation step using a wafer A 121 and an active step using a wafer B 122. The wafer A 1221 and the wafer B 122 refer to the use of distinct wafers rather than two specific wafers. In the preparation step, it would be desirable to use a small number of wafers A 121 while collecting as large a number of defect samples as possible. Thus, it would be preferable to use multiple wafers rather than just one. Also, it would be preferable to have these multiple wafers drawn from separate lots. Also, the wafers A and the wafers B can be of different types as long they are produced using similar processes.

The following is a description of the flow of operations in an example using the wafer A 121.

When the wafer A 121 is sent to the production process, the processes indicated by the circles in Fig.3 are performed successively. A circuit pattern is formed by repeating film formation processes 1, 3, 4, exposure process 6, and etching 7. In addition, there are ion implantation, cleaning, and other processes, but these are not shown in the figure.

Inspections, indicated by diamonds in Fig.3, are performed between the main processes. In particular, contaminant inspection processes 2, 5 are performed after film formation processes, which generate a lot of contaminants. Also, visual inspection process 8, which can detect pattern defects, is performed after the circuit pattern is formed by the etching process 7. In this inspection, contaminants on the wafer surface and circuit pattern deformations are detected by an automated inspection device. The position information for these detected contaminants and circuit pattern deformations is output in the form of coordinate data.

However, defects detected by the automated inspection device will not necessarily be critical defects having electronic significance. Some of the defects may be

discoloration defects and contaminant defects which are electronically functional and not critical defects. Thus, selecting the critical defects out of the detected defects becomes important. While it would be desirable to perform inspections before and after each individual process, inspections are carried out only after the main processes. This is due to restrictions related to production times and inspection costs. Once the electronic circuit is completed after all the processes are finished, an electronic test is performed to check electronic operations.

This inspection system allows detection of critical defects generated in processes before the wafer is completed. By taking measures in response to these defects, faults in the subsequently produced wafer B 122 can be minimized. The semiconductor device production process shown in Fig.3 will be described in detail, with references to Fig.4.

Fig.4 is a flowchart illustrating the sequence of operations used in an inspection according to this embodiment. The following is a description of the specific implementation steps based on Fig.4 and with references to Fig. 1 and Fig.3. In the flowchart in Fig.4, there is a preparatory step using the wafer A 121 and the active step using the wafer B 122. In the description below, defect images are used as an example of detailed defect information.

(1) Defect inspection

In Fig.4, defect inspection 131 corresponds to the visual inspection process 8 from Fig.3. At this stage, the wafer A 121 from Fig.3 has passed through the processes 1, 3, 4, 6, 7 and contaminant inspection processes 2, 5, and has reached the visual inspection process 8. The visual inspection process 8 is performed after the circuit pattern has been formed by the etching process 7, so the effect of defects on the circuit pattern can be determined. The visual inspection process 8 is performed by the inspection device 100 from Fig. 1. The coordinate data output (defect map) is sent to the defect data management server 103 by way of the network 104 and is stored in the

storage device 108.

(2) Sampling

In Fig.4, a sampling step 132 samples defects for which detailed information is to be collected using the defect map from the visual inspection process 8. Since the inspection device 100 performs high-speed inspection, digital images of the wafer surface with a low resolution are used. The low-resolution digital images allow the presence of defects to be determined, but collecting detailed information that can accurately identify the appearance of the defect and the like is difficult. Thus, after inspection, detailed information must be collected by capturing a finer digital image of a defect or the like. Since the high-resolution digital images are captured by moving the wafer successively, the time required is proportional to the number of defects.

Since several hundreds to several thousand defects may be detected on the wafer by the inspection device 100, these must be narrowed to less than a hundred coordinate points to allow fine digital images to be captured within a limited amount of time. In the sampling operation, the defect data management server 103 from Fig. 1 reads a defect map from the storage device 108 and sends the map to the review device 101 by way of the network 104. The sampling operation will be described in detail later.

(3) Image retrieval

An image retrieval step 133 shown in Fig.4 corresponds to the process 8' from Fig.3 and involves recording fine digital images of the sampled coordinates. This is one example of how detailed defect information can be collected. Alternatively, methods such as collecting EDX analysis curves can be used to collect detailed defect information. Image retrieval is performed by the review device 101 from Fig. 1. The inspection device 100 moves the wafer to align it. The sampled coordinate data 105 is received from the defect data management server 103 by way of the network 104, and the stage is moved to the defect position using the coordinate data. A defect image is

then captured. The captured defect image 106 is sent to the defect data management server 103 by way of the network 104 and is stored in the storage device 108 in association with defect coordinates.

(4) Electronic testing

An electronic testing step 134 in Fig.4 corresponds to a process N from Fig.3 and is an electronic inspection performed after the wafer A 121 has passed through the predetermined processes. This step is performed by the electronic tester 102 from Fig. 1. Coordinate data for electronic faults and position data for defective chips are sent to the defect data management server 103 by way of the network 104 and are stored in the storage device 108.

(5) Coordinate consistency checking

In a coordinate consistency checking step 135 in Fig.4, the results from the defect map and the electronic test are compared to study consistencies and inconsistencies between the two. A defect map and test results from the storage device 108 in the defect data management server 103 from Fig. 1 are stored in memory and used. The results of the consistency check are stored in the storage device 108 as electronic data, to be described later.

Fig.5 shows an example of a consistency checking operation. In this figure, a map of failed bits is compared with a defect map. Precise faulty bit positions 154 are recorded on the map of failed bits and comparing these with defect coordinates provides an accurate evaluation of the criticality of individual defects.

The evaluation of whether a faulty bit matches a defect is performed by determining a match when the two points are closer than a predetermined distance. This distance is the margin of error for defect coordinates output by the inspection device 100 and can be measured beforehand. This distance is entered in the defect data management server 103 from Fig. 1 beforehand.

Instead of a map of failed bits, it is also possible to use electronic test results

from a short-circuit checking TEG (Test Element Group). The short-circuit checking TEG is a striped dummy pattern formed with the same process as used in the product. By measuring the electronic characteristics of the ends of the stripes, short-circuits or circuit breaks can be detected. By comparing the striped areas containing short-circuits or circuit brakes with defect coordinates, electronically critical defects can be identified.

Fig.6 shows the stored results of the coordinate consistency checking operation. The coordinate consistency checking operation is performed in the defect data management server 103 from Fig. 1 and results are stored in the storage device 108 using the data structure shown in Fig.6. In this figure, a defect number 160 is an identification number assigned to defects by the inspection device 100. Chip coordinates 161 are coordinates of a chip containing a defect. Defect coordinates 162 are coordinates of defects relative to coordinate systems where the origins are located at a predetermined point on each individual chip. In the data structure in Fig.6, if the defect number 160 is specified the chip coordinates 161 and the defect coordinates 162 can be used to calculate a defect position to move to.

A sampling flag 163 is a flag identifying a defect selected by the sampling operation. In the example shown, '1' indicates a selected defect and '0' indicates a defect that was not selected. An image name 164 is a name of an image captured by the review device 101 and is available only for defects having a sampling flag of '1'. The test result 165 indicates whether the evaluation results for the electronic test performed on the chip containing the defect is Good or Not good ('G'/'N').

In the example in this figure, G is entered if a defect does not match a region evaluated negatively by the electronic test. In the format shown in this figure, defects showing an 'N' as the test result and a '1' as the sampling flag are collected to categorize critical defect images, and defects showing a 'G' as the test result and a '1' as the sampling flag are collected to categorize non-critical defect images.

(6) Display image

In an image display step 136, image associated with coordinates are displayed based on the results from the coordinate consistency checking operation. This is a first characteristic of the present invention. The defect data management server 103 from Fig. 1 reads defect image data and coordinate consistency data, shown in Fig.6, from the storage device 108. The coordinate consistency data is referred to, and defect images are displayed on the display device 109.

Fig.7 shows examples of displayed images. Fig.7 (a) shows optical microscope images, arranged in the order that they were captured, of defects generated in the aluminum wiring process for the semiconductor device.

Fig.8 shows a screen 1091 in which the optical microscope image of the defect is displayed on the display device 109. A defect image 2111 corresponds to the image of all defects shown in Fig.7 (a) and is associated with the pre-classification defect image 211 retrieved by the review device 101 shown in Fig. 14. The operator enters a product name 220, a lot number 221, a wafer number 222, and a process name 223 in the screen 1091. Based on this information, the defect coordinates and the fault coordinates 212 and the defect images 211 for this wafer are searched from the storage device 108. The results are displayed on the screen 1091 of the display device 109 as a defect map 2101, a map 2121 of failed bits (one type of fault map), and a defect image 2111.

In addition to aluminum wiring processes, the following description will apply in a similar manner to wiring production processes such as gate wiring. In Fig.7 (b), critical and non-critical defects are classified by manually estimating electronic criticality from the image characteristics. The classification is performed by having the operator observe the images on the display device 109, visually evaluate criticality/non-criticality, and operate the input device 110.

In the example shown in Fig.7 (b), a defect in which a contaminant 171

short-circuits a circuit pattern 170 is assessed as being critical. If there is no short-circuit, the defect is assessed as non-critical. However, whether a contaminant disposed between two patterns 170 (e.g., a contaminant 172) is conductive or non-conductive is difficult to determine from images, so the validity of Fig.7 (b) is not definite.

Fig.7 (c) shows displayed images of the results of the coordinate consistency checking by clicking a coordinate consistency checking button 224 on the display screen 1091 in Fig. 8. If the test result from the consistency data in Fig.6 is 'G', the defect image is displayed as a non-critical defect. If the test result is 'N', the defect image is displayed as a critical defect.

One advantage of the display shown in Fig.7 (c) is that the critical defects and non-critical defects can be accurately classified using the coordinate consistency checking results. There are many types of defects generated in the production process for semiconductor devices, and the image characteristics for these are also varied. Thus, when assessing criticality of defects from image characteristics, it is difficult to determine which image characteristics should be emphasized.

However, with the image display provided by the present invention, defect criticality can be assessed with guidelines on what image characteristics should be studied. This allows more accurate criticality evaluations to be made. By comparing similarities between image characteristics of critical defects and differences between image characteristics of critical and non-critical defects, it is possible to determine image characteristics that can be used to accurately evaluate critical defects. As a result, the number of critical defects can be determined accurately by examining these image characteristics and classifying the defect images.

Furthermore, carefully analyzing the image characteristics of critical defects can provide an estimation on the cause of the critical defects. Also, even if no significant differences between critical and non-critical defects can be observed in the

image characteristics, this indicates that distinguishing the two based on images is difficult and unnecessary classification operations can be omitted.

The following is a detailed description of the above embodiment, with references to Fig.7 (c). Comparing Fig.7 (c) and Fig.7 (b), it can be seen that the short-circuit between the contaminant 172 and the pattern 170 is not relevant to criticality. However, it can be seen that the image of the critical defect (the contaminant 171) is dark and large. The images of non-critical defects (the contaminant 172 and the contaminant 182) are either relatively light or, even if they are dark, small.

Furthermore, by analyzing the image characteristics in each of the categories, an estimation of the causes of the defects can be made, as shown in Fig.9. Fig.9 shows cross-section drawings of the defects from Fig.7(c). The prominently projected contaminant is dark since it scatters the illuminating light more. The shorter contaminants scatter light to a lesser degree and therefore result in lighter images.

In Fig.9 (a), a dark contaminant 177 is projected prominently so that it breaks through an insulative layer 170, leading to a critical defect with a short-circuit or pattern break in the pattern 170 and a base pattern 180. On the other hand, since a light contaminant 178 shown in Fig.9 (b) has less height, there is no short-circuit in the pattern 170 and the pattern 180, resulting in a non-critical defect. Also, in Fig.9 (c), a dark, small contaminant 181 does not lead to short-circuits or broken patterns due to its size, thus resulting in a non-critical defect.

Based on this, the prominently projected contaminant 177 is a critical defect in this process and setting up a fault prevention measure would be useful. For example, the thickness of the insulative layer 179 could be temporarily increased to prevent short-circuits between the upper pattern 170 and the base pattern 180. Also, more fundamentally, the material of the critical contaminant can be analyzed to determine where it is being generated.

(7) Classify image

If, using the displayed images from step (6) described above, significant image characteristic differences are found between critical and non-critical defects, classification can be automated using an ADC device. To automate classification using an ADC device, the classification device must be trained. By clicking a training button 225 displayed on the screen 1091 in Fig. 8, training is carried out based on the results from the displayed images from step (6) above, the accuracy with which critical defects are classified can be improved. This is a second characteristic of the present invention.

In an image classification step 137 shown in Fig.4, the operator of the defect data management server 103 from Fig. 1 observes the image display results on the display device 109 and operates the input device 110. The results of the operations are received by the defect data management server 103 are added as new information to the coordinate consistency checking data in Fig.6 and stored in the storage device 108.

The following is a description of image classification operations suited for ADC training, with references to Fig.10. Fig.10 (a) is identical to Fig.7 (c). It is important to note here that image characteristics within the critical defect and non-critical defect categories will not all be the same. Defects leading to electronic faults are caused by different things and these will involve different visual characteristics. The same thing can be said for non-critical defects.

Thus, to train the ADC device, the critical defects and non-critical defects must be categorized further to provide the same image characteristics within the categories. For example, the critical defects in Fig.10 (a) are all dark contaminants 182. However, examining the image characteristics of non-critical defects shows that there are both light contaminants 183 and dark contaminants 184. For this reason, the non-critical defect category must be sub-divided.

To do this, a pointing device (not shown in the figure) is used to indicate the frame for the category to be sub-divided, as shown using the thick frame in Fig.10 (b). Next, frames for the new sub-divided categories are created on the screen, as shown in

Fig.10 (c). This corresponds to the bright defects and dark defects shown in this figure. Next, the images in the non-critical defect frame are dragged using the pointing device to the bright defect or the dark defect frame. As shown in Fig.10 (d), this allows the non-critical defects to be divided into two categories.

Fig.11 shows an example of electronic data containing the results from the image classification operation described above. This electronic data is stored in the memory of the defect data management server 103 by way of the network 104 and is updated as the screen of the display device 109 changes. The data in Fig.11 is similar to the data shown in Fig.6, with the addition of a image classification field 174. When a defect on the screen is selected with the pointing device or the like, the corresponding defect number is identified by the defect data management server 103 from Fig. 1. As the image on the screen is moved, the content of the image classification field 174 in the electronic data shown in Fig.11 is updated.

In the embodiment described above, the sub-dividing of critical defects or non-critical defects is performed manually based on a screen display. However, it would also be possible to perform this operation automatically through a known statistical classification method known as clustering, which does not involve training (Okuno, et. al., Multivariate analysis, 1971, Nikkagiren Shuppansha, pp. 391 - 412).

(8) Criticality evaluation

A criticality evaluation step 141 shown in Fig.4 and Fig.3 evaluates whether or not the classification results from the ADC device correctly reflect criticality. This is a third important characteristic of the present invention.

The operation is performed in three steps: (a) a defect classification operation; (b) a coordinate consistency checking operation; and (c) a criticality calculation operation. In the defect classification operation (a), the defect data management server 103 from Fig. 1 reads into memory a defect map and an associated defect image stored in the storage device 108. The classification device 111 classifies the defect image and

stores the classification results as electronic data, which is then stored in the memory in the defect data management server 103.

The classification results are stored in association with the defect coordinates 162, as shown in Fig.11. In the coordinate consistency checking operation (b), The defect data management server 103 reads into memory the electronic test results for the position corresponding to the defect coordinates stored in the storage device 108. Coordinate consistency checking is then performed to determine if there is a match with the defect coordinates. In the criticality calculation operation (c), the match rate between the defect coordinates and the electronic test results are tabulated for each of the image classification categories. A criticality rate KR, which is a value used for evaluation, is calculated as shown below. According to this definition, criticality increases as KR approaches 1, and criticality decreases as KR approaches 0.

$$KR=N_N/N_O \qquad \text{Expression (1)}$$

In expression (1), N_N is the number of defects where the fault position on the map of failed bits matches defect map coordinates. N_O is the number of defects in the defect map.

By using this criticality rate, the operator can determine whether or not to redo the image classification operation (the image reclassification branch 139 in Fig.4), and can determine whether a criticality evaluation based on defect images is possible (the criticality determination branch 140 in Fig.4).

First, the decision of whether or not to redo image classification will be described. The following criticality rates are used to determine whether or not critical defects and non-critical defects have been properly classified.

$$KR1= N_{N1}/N_{O1} \qquad \text{Expression (2)}$$

$$KR2= N_{N2}/N_{O2} \qquad \text{Expression (3)}$$

Here, criticality rate KR1 is the criticality rate for defects classified as being critical. N_{N1} is the number of defects in which the defect map matches the coordinates on the

map of failed bits. No 1 is the number of defects classified as critical in the defect map. Similarly, KR2 is the criticality rate of defects classified as non-critical defects.

KR1 and KR2 are calculated by the defect data management server 103 from Fig. 1 and are displayed on the display device 109. The operator checks the display results and decides whether or not to re-do the image classification operation. If KR1 and KR2 do not approach ideal values even after re-doing the image classification operation, the operator decides that criticality is difficult to evaluate from defect images and stops image-based criticality evaluations.

Fig.12 shows sample criticality rate calculation results. In the example in Fig.12 (a), classification of critical/non-critical defects was not performed properly. In Fig.12 (b), the classification was performed properly. In these figures, the horizontal axis represents defect categories 190 and the vertical axis represents a criticality rate 191. The maximum value for the criticality rate is 1.0. Regarding Fig.12 (a), the difference between the criticality (KR1) for critical defects, 0.6, and the criticality (KR2) for non-critical defects, 0.4, is small, and KR1 is much less than the maximum possible criticality value of 1.0. This indicates that classification of critical defects was not performed properly. On the other hands, the results in Fig.12 (b) indicate that KR1 is 1.0, which is the maximum possible criticality value. This indicates that proper classification was performed.

With the present invention, an accurate, quantitative assessment can be made of criticality based on the results of image classification. This allows the operator to know whether image classification should be re-done or not and allows efficient defect analysis. Furthermore, since the operator can assess whether criticality evaluation based on defect images will be difficult or not, unnecessary defect analysis operations can be skipped.

(9) Criticality evaluation

A criticality evaluation step 141 shown in Fig.4 and Fig.3 is performed by the

defect data management server 103. Once the preparatory step using the wafer A 121 is completed and it has been determined based on the criticality evaluation step 138 that critical defects can be classified, then the active step for the wafer B 122 is begun.

A specific example will be described, with references to Fig.3. When the electronic testing of the wafer A 121 has been completed, a wafer which has not reached the visual inspection process 8 serves as the wafer B 122. In the preparatory stage, the image characteristics of critical defects are determined at the visual inspection process 8. Thus, when the wafer B 122 reaches the visual inspection process 8, defects are imaged and their images 2111 in Fig. 8 are collected. Then, clicking a criticality evaluation button 226 displayed on the screen 1091 in Fig. 8, critical defects are classified based on these image characteristics. Furthermore, the criticality rates of each of the classified categories has been determined.

In the present invention, the basis for image classifications is associated with the actual electronics testing results, and the degree of correlation is quantified as a criticality rate. As a result, the number of electronic faults determined after wafer completion for a conventional wafer A 121 can be predicted with high accuracy at the visual inspection 8 during the processing of the wafer B 122. As a result, yield can be predicted during an intermediate process and prevention of defects can be started earlier.

The method used to predict yield will be described. Defects can generally be classified as those generated in a concentrated manner and those generated randomly. In the present invention, the classification results for a set of defects selected by sampling can be used for overall predictions. This is suited for random defects. Yield from random defects can, for example, be calculated using the following equation.

$$Y=1-T/T_0 \qquad \text{Expression (4)}$$

Here, Y represents the predicted yield, T represents the number of chips containing defects, and T_0 represents the number of inspected chips. However, since not all

defects detected by the inspection device will necessarily be critical, criticality can be taken into account. Thus, expression (4) becomes the following equation.

$$Y_i = 1 - KR_i * T_i / T_0 \qquad \text{Expression (5)}$$

Here, Y_i represents the yield based on category i, KR_i represents the criticality of category i, T_i represents the number of chips containing defects classified as category i by the ADC device, and T_0 represents the number of inspected chips.

Fig.13 shows examples of yield predictions during intermediate processes when expression (5) is used in the present invention. The horizontal axis in the figure represents inspection processes and the vertical axis represents the number of defects or yield decreases. In process m in the figure, the number of defects determined by the ADC device to be critical is 21 and the number of non-critical defects is 26. A yield reduction rate DYL can be calculated using expression (5) as follows.

$$DYL = 1 - Y$$

$$= KR_i * T_i / T_0$$

$$= 1.0 * 18 / 257 = 7.0\% \qquad \text{Expression (6)}$$

Of the 21 critical defects, three overlap with other critical defects in the same chip. Thus, the number of chips T_i containing defects is 18. Compared to the conventional method of visual classification, the present invention allows yield to be calculated accurately. As a result, the presence of critical defects can be recognized quickly and accurately so that the defects to be considered for fault prevention can be determined accurately.

Next, a method for using the yield calculation results described above for fault prevention will be described with references to Fig.13 and Fig.14. Once critical defects are discovered, it is important to identify the causes and especially the processes during which the defects were generated. This allows the focus for critical defect prevention to be narrowed and minimizes defects by preventing critical defects from being generated. The coordinate consistency checking operation shown in Fig.14

is used to identify the process in which a critical defect was generated. For example, defect inspections are performed more often in the processes prior to process m for individual wafers. If, for example, a dark-field inspection device capable of performing high-speed inspections is used for the inspection device 100, frequent defect inspections for processes prior to process m can be performed without delaying the processing of the product.

By checking for consistency between contaminant inspection results 201, 202 and visual inspection results 203 for the same wafer, it is possible to determine the contaminant-generating process that resulted in a visually detected defect. Fig.13 shows the results of how the defects classified as critical defects in the visual inspection process m are broken down in the contaminant inspections for the twelve processes a through l. Thus, for the twelve processes, the frequencies at which defects leading to critical defects at process m are generated can be compared, and processes having relatively high critical defect generation frequencies can be identified. In the example shown in Fig.13, both process f and process h have a high number of defects, but process f has a higher proportion of critical defects, indicating that it should be given priority. This embodiment takes advantage of the characteristic of the present invention that critical defects can be accurately evaluated. If these operations were performed based on inaccurate critical defect classification resulting from conventional visual classification, an erroneous process would be identified as the process generating critical defects, thus preventing effective measures to be taken.

When identifying critical defect generation using the consistency checking operation described above, efficiency can be improved by performing sampling as indicated in Fig.15. The logical sum is taken for the multiple defect maps obtained from inspecting the twelve processes a through l (e.g., inspection results 2; 203 and inspection results 5; 204). Then, at process m (visual inspection) a sampling operation 206 is performed for the defects resulting from this logical sum. As a result, the

criticality/non-criticality evaluation for sampled defects will always allow the process generating the defects to be identified.

As described above, the present invention uses an ADC device to automatically categorize defects and allows highly accurate yields to be calculated using defect counts by categories and criticality rates by categories. Also, these operations can be performed before the electronic testing process is reached. Thus, compared to conventional technologies, yield decreases and the processes at which yield-reducing defects are generated can be identified earlier during the N days between the visual inspection and the electronic testing (generally 10 - 90 days depending on the visual inspection process). Thus, fault prevention measures can be implemented efficiently at an early stage and defective products can be minimized.

In the example described above, the wafer A and the wafer B are identical wafer types. However, different types can be used if the production methods are similar. Taking semiconductor devices as an example, different products are frequently produced using similar processes. Since defects are often specific to processes, if critical defect classification guidelines are made clear using a certain type of wafer A, then a wafer B produced using a similar process can have critical defects accurately evaluated beginning with the start of production.

In the embodiment described above, classification guidelines are determined after the test results for the wafer A 121 have been determined. However, it would also be possible to predict critical defects using images of the wafer A 121 and determine provisional classification guidelines before the wafer A 121 reaches the electronic testing step. Once the wafer A 121 reaches the electronic testing step, classification guidelines can be reexamined according to the embodiment described above.

Furthermore, the preparatory stage with the wafer A 121 can be omitted and operations can be carried out solely for the active stage with the wafer B 122. If critical defects can be clearly determined from the detailed defect information, criticality can

be assessed using the detailed defect information before the wafer reaches the electronic testing step. Defect analysis using the critical defect count can be performed as shown in Fig.12.

In the first characteristic of the embodiment described above, guidelines are determined to establish the detailed information to focus on when evaluating criticality for different types of defects such as those generated in semiconductor production processes. This allows more accurate criticality evaluations. Since the relation between the detailed defect information and electronic criticality is made clear through objective data operations, classification guidelines for accurately classifying critical defects can be provided.

Another characteristics of the embodiment described above is that a quantitative assessment of whether critical defects have been accurately determined is possible. Thus, a decision can be made on whether to re-evaluate critical defects or not. This allows efficient defect analysis. Furthermore, since a determination can be made on whether criticality evaluation based on the detailed defect information is difficult or not, unnecessary defect analysis operations can be skipped, thus allowing more efficient defect analysis.

Another characteristic of the embodiment described above is that defect criticality, which was determined after completion of the wafer in the conventional technology, can be evaluated in a precise manner in the visual inspection step, which is an intermediate process. Thus, analysis can be performed with higher priority being given to defects generated by yield-reducing factors that lead to high electronic criticality and high frequency of occurrence. This allows fault prevention measures to be started early.

Another characteristic of the embodiment described above is that a criticality rate can be quantitatively determined to indicate correlation between the detailed defect information and the actual electronic testing results as well as the degree of this

correlation. As a result, yield, which is determined after wafer completion in the conventional technology, can be accurately determined at a stage before completion. This allows early evaluation of whether or not a required number of working products can be completed in time for a shipping date. By taking measures such as increasing production input, loss of sales opportunities can be prevented beforehand.

Another characteristic of the embodiment described above is that faults detected at the completed stage of the inspected object can be accurately predicted from defects detected in the production process. Thus, prevention of significant defects can be undertaken without having to wait for the final inspection after completion of the product. This allows yield to be improved at an early stage.

Another characteristic of the embodiment described above is that faults detected at the completed stage of the inspected object can be accurately predicted from defects detected in the production process. Thus, prevention of significant defects can be undertaken without having to wait for the final inspection after completion of the product. This allows yield to be improved at an early stage.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiment is therefor to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.